

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-039866

(43)Date of publication of application : 05.02.2004

(51)Int.Cl.

H01L 21/8247
H01L 27/10
H01L 27/115
H01L 29/788
H01L 29/792

(21)Application number : 2002-195005

(71)Applicant : TOSHIBA CORP

(22)Date of filing : 03.07.2002

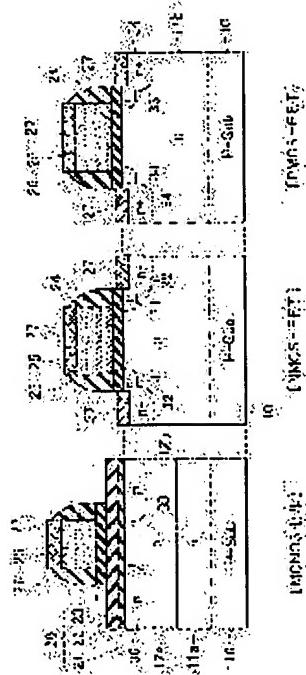
(72)Inventor : AIDA AKIRA
NOGUCHI MITSUHIRO
TANAKA MASAYUKI
SAIDA SHIGEHIKO

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device of high performance wherein a MONOS type memory cell is formed on a semiconductor substrate and a method for manufacturing the device.

SOLUTION: This semiconductor device is provided with the semiconductor substrate, the memory cell which is formed on the semiconductor substrate and has a first gate insulating film of a laminate structure which contains a silicon nitride film turning to a charge storage layer, and a transistor which is formed on the semiconductor substrate and has a second gate insulating film. A source/drain diffusion layer of the memory cell is coated with a part of the first gate insulating film, and a metal silicide film is formed on a surface of a source/drain diffusion layer of the transistor.



LEGAL STATUS

[Date of request for examination] 15.07.2003

[Date of sending the examiner's decision of rejection] 19.04.2005

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of
rejection]

[Date of requesting appeal against examiner's
decision of rejection]

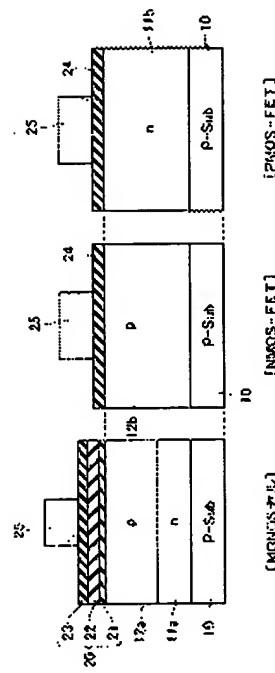
[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

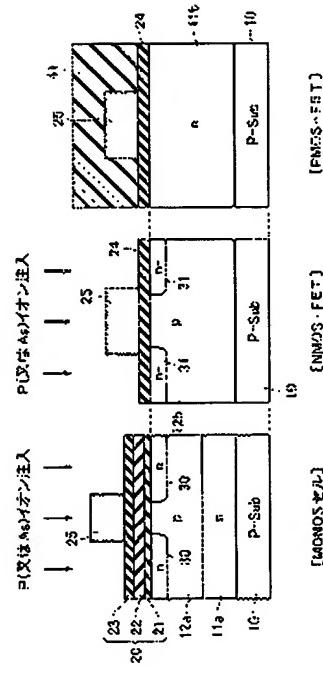
(15)

JP 2004-39866 A 2004.2.5

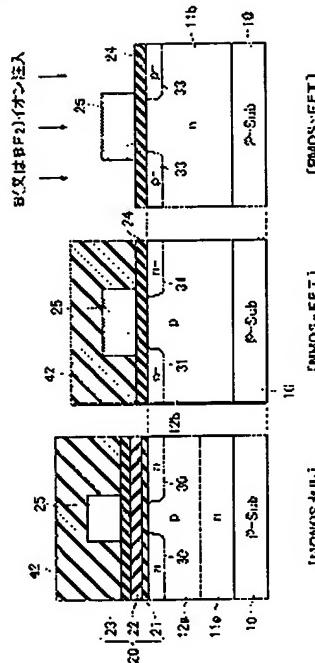
【図 3】



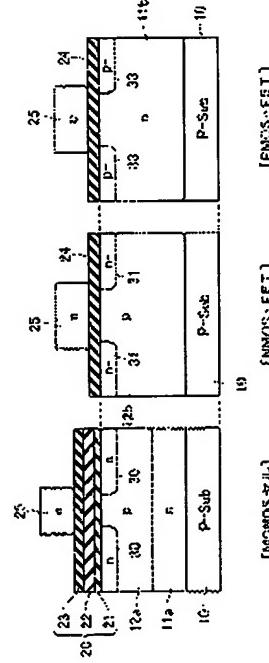
【図 4】



【図 5】



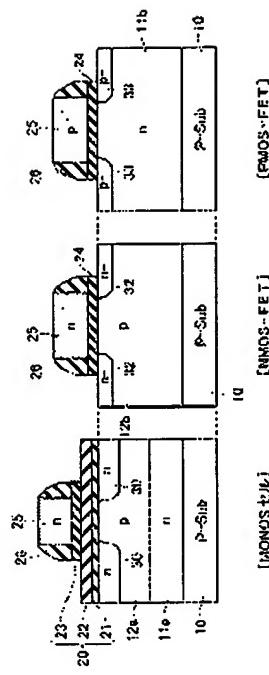
【図 6】



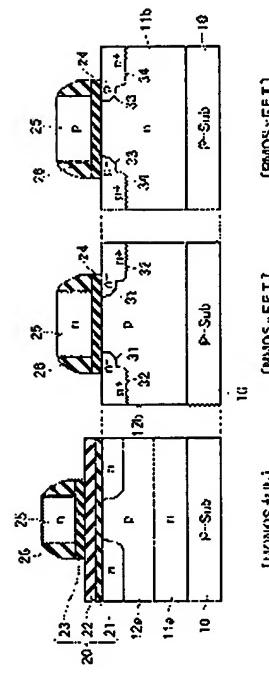
(15)

JP 2004-39866 A 2004.2.5

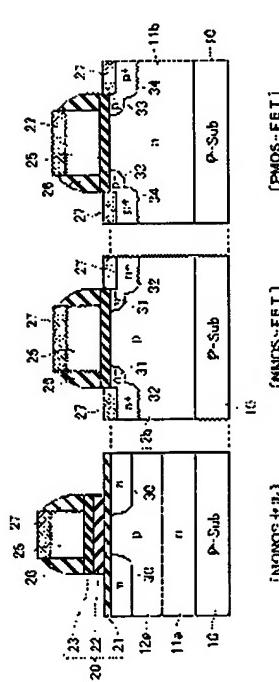
[図7]



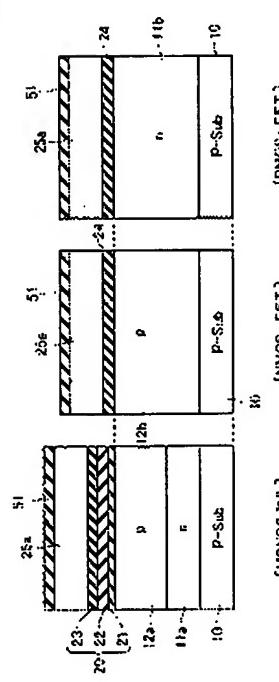
[図 8]



[図 9]



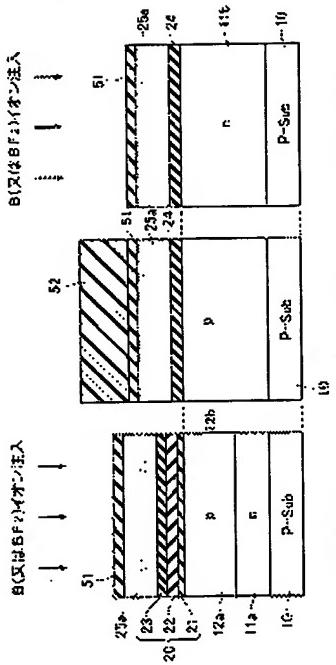
[図 10]



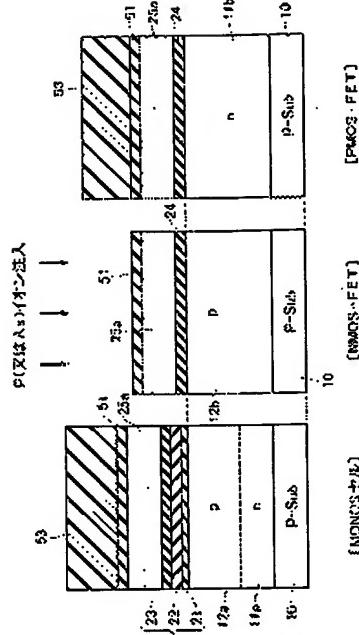
(12)

JP 2004-39866 A 2004.2.5

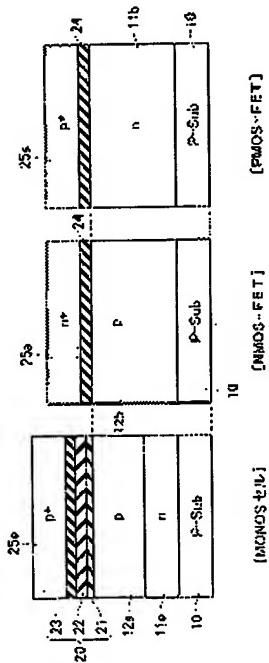
【図 1 1】



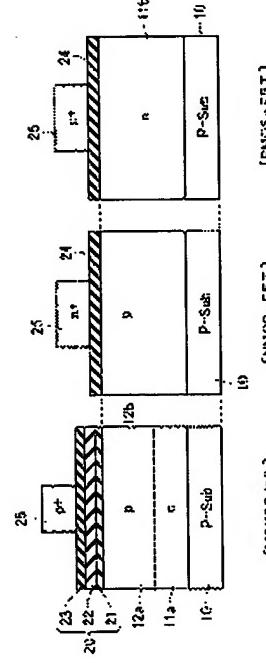
【図 1 2】



【図 1 3】



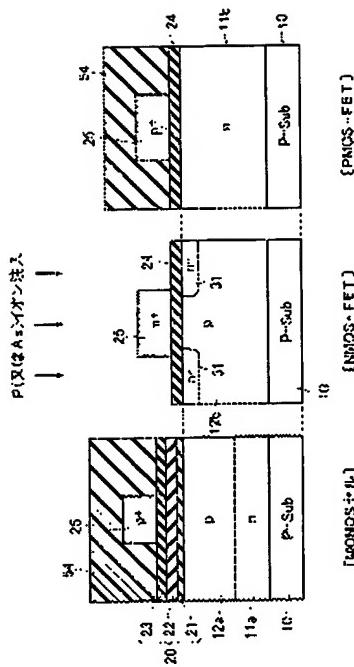
【図 1 4】



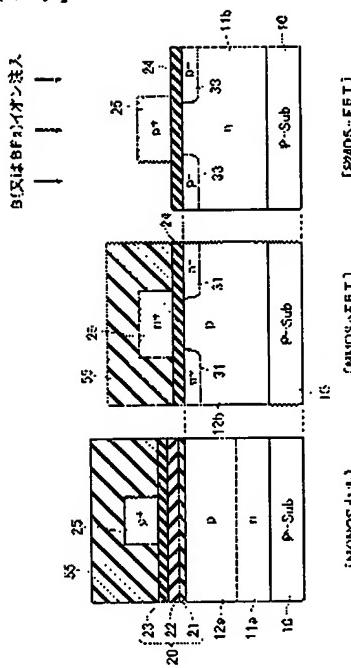
(18)

JP 2004-39866 A 2004.2.5

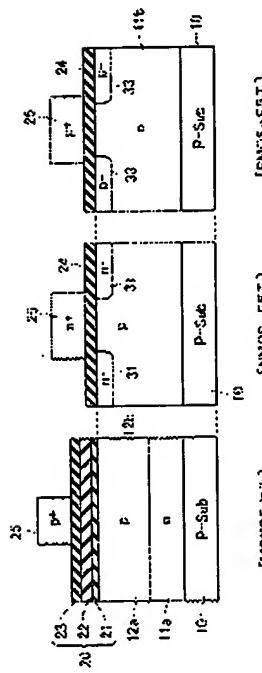
【図 15】



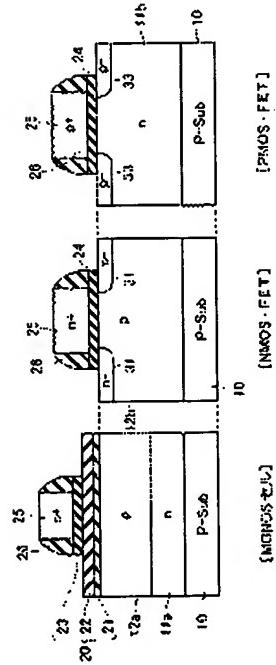
【図 16】



【図 17】



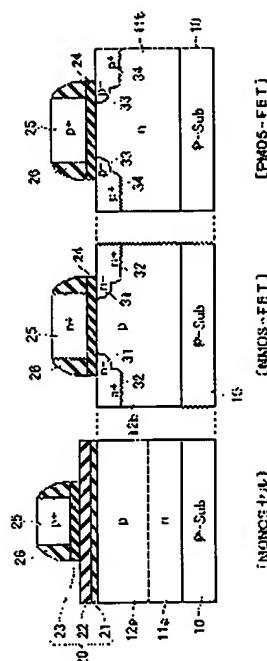
【図 18】



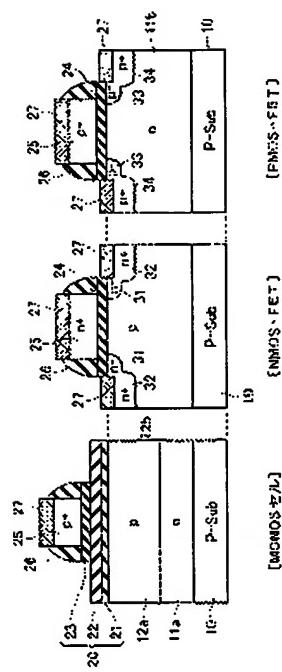
(19)

JP 2004-39866 A 2004.2.5

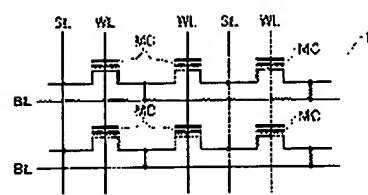
[図 19]



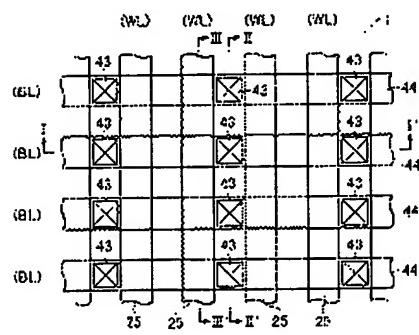
[図 20]



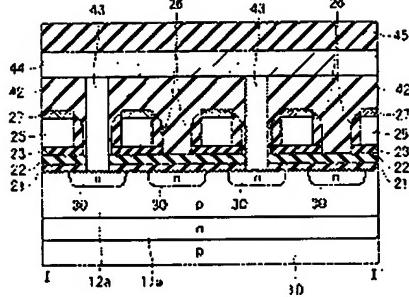
[図 21]



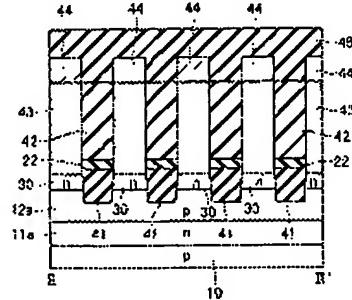
[図 22]



[図 23 A]



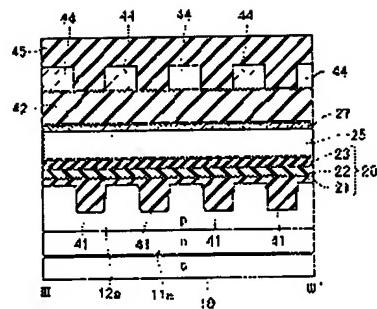
[図 23 B]



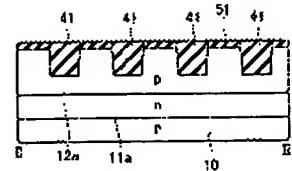
(30)

JP 2004-39866 A 2004.2.5

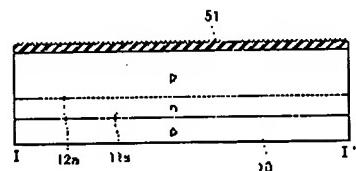
【図 23 C】



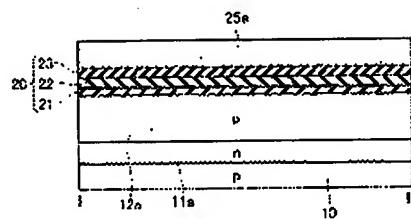
【図 24 B】



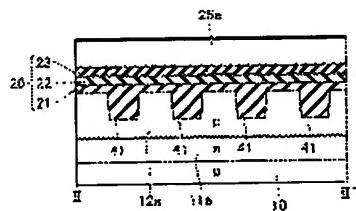
【図 24 A】



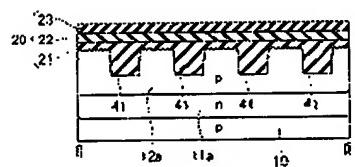
【図 25 A】



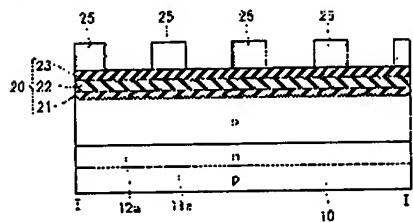
【図 25 B】



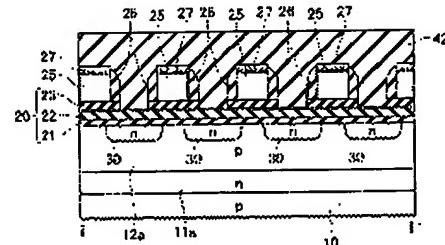
【図 26 B】



【図 26 A】



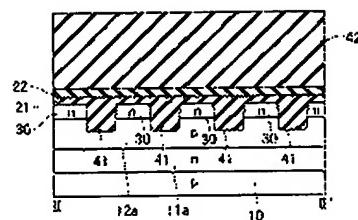
【図 27 A】



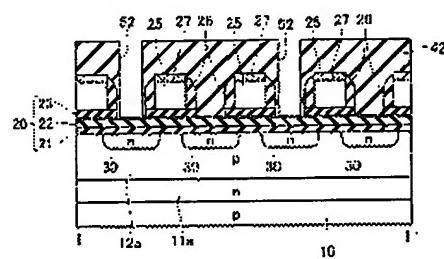
(21)

JP 2004-39866 A 2004.2.5

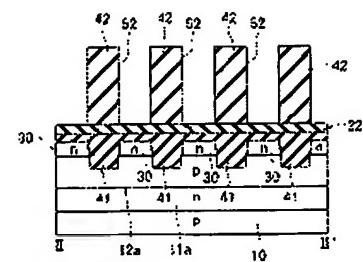
【図 27B】



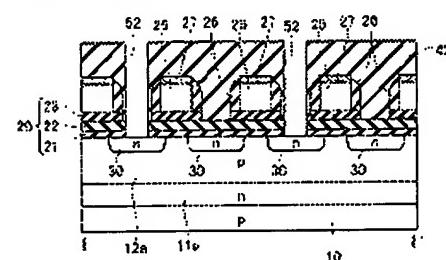
【図 28A】



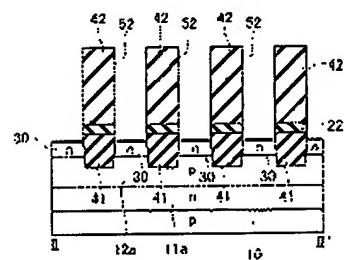
【図 28B】



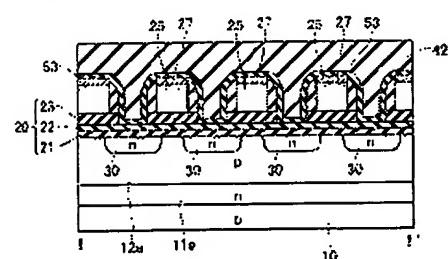
【図 29A】



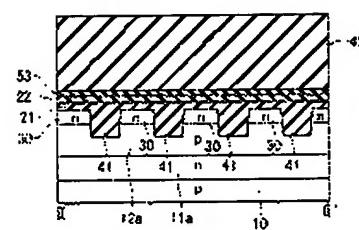
【図 29B】



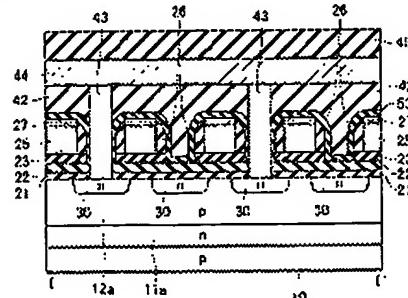
【図 30A】



【図 30B】



【図 31A】



(22)

JP 2004-39866 A 2004.2.5

【図31B】

